(19) Europäisch s Patentamt
European Patent Office
Office europ´ n des brevets

(11) Publication number: **0 303 435**
A2

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: **88307335.5**

(22) Date of filing: **08.08.88**

(51) Int. Cl.[4]: **H 01 L 29/52**
H 01 L 29/60

(30) Priority: **11.08.87 JP 199006/87**

(43) Date of publication of application:
15.02.89 Bulletin 89/07

(84) Designated Contracting States: **DE FR GB NL**

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(54) **Bipolar transistors.**

(57) A bipolar transistor comprises a buried collector region (12, 22), a base region (20/23) and an emitter region (21) formed in a device forming region (13) surrounded by an isolation region (14). A base contact electrode (15) and a collector contact electrode (16) are arranged in symmetry with each other. The collector contact electrode (16) is formed through an opening (10) formed in a portion of the isolation region (14) for connection with the buried collector region (12, 22). This enables collision between the base region (20/23) and a collector contact region (22) of the buried collector region (12, 22) to be avoided effectively.

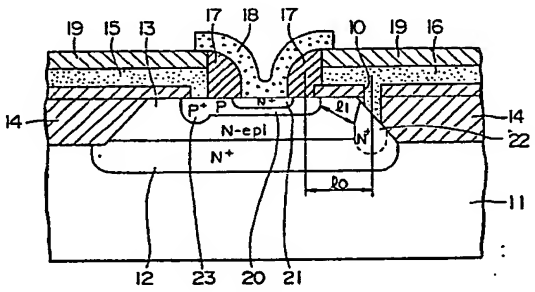

FIG.1

EP 0 303 435 A2

Description

BIPOLAR TRANSISTORS

This invention relates to bipolar transistors.

It has previously been proposed to employ a structure, for a bipolar transistor that is to operate at an extremely high speed, in which base contact and collector contact are achieved by arranging for a base contact electrode and a collector contact electrode to extend into a device forming region from an end of a region delimited or surrounded by an isolation region.

Figure 6 of the accompanying drawings shows in cross-section such a bipolar transistor in which the base contact electrode is arranged in symmetry with the collector contact electrode. An N^+ type buried collector region 102 is formed on a semiconductor substrate 101 and an N type epitaxial layer 103 is formed onthe collector region 102. An isolation region 104 is formed so as to surround the layer 103. The N type epitaxial layer 103 serves as a device forming region. An N^+ type collector contact region 108a and an N type collector contact region 108b for electrical connection with the buried collector region 102, a P type intrinsic base region 109, a graft base region 110 and an emitter region 111 are formed within the N type epitaxial layer 103. A base contact electrode 106 and a collector contact electrode 107, covered by an insulating layer, are formed in an opening region 105 on the surface of the N type epitaxial layer 103 in symmetry with each other. A thin polycrystalline silicon layer 112 is formed on the insulating layer covering the contact electrodes 106 and 107.

The collector of the above-described bipolar transistor is connected by way of the buried collector region 102, the N^+ type collector contact region 108a and the N type collector contact region 108b to the collector contact electrode 107, while the base of the transistor is connected by way of the intrinsic base region 109 and the graft base region 110 to the base contact electrode 106.

In the above-described bipolar transistor, the following problems are encountered in connection with the transistor characteristics.

With reduction or shrinking of the dimensions of the device components, the spacing or interval between the intrinsic base region 109 and the N type collector region 108b is reduced. In such a case, the P type intrinsic base region 109 and the N type collector contact region 108b can collide with each other, thus resulting in a reduced collector to base breakdown voltage and an increased parasitic capacitance.

On the other hand, it is desirable to increase the impurity concentration of the N type collector contact region 108b in order to lower the resistance of the region 108b. However, it is of necessity not possible to lower the collector resistance since the impurity regions again may collide with each other if the impurity concentration is increased.

Respective different aspects of the invention ar set forth in claims 1, 7 and 8.

According to another aspect of the invention, a bipolar transistor has a buried collector region, a base region and an emitter region in a device forming region delimited or surrounded by an isolation region. The emitter region is isolated by a side wall insulating layer on a major substrate surface. The base region is connected to the base contact electrode by way of a graft base region. The buried collector region is connected to a collector contact electrode arranged in symmetry with the base contact electrode with respect to the emitter region. The collector contact electrode is connected to the buried collector region by way of an opening formed at at least a portion of the isolation region. In a manner distinct from an opening formed previously by selective oxidation, the opening is formed through an isolation region after formation of the isolation region. By making a connection by way of this opening, a larger distance is provided between the base region and the collector contact region to avoid collision between the impurity regions.

According to a further aspect of the invention, a process for making a bipolar transistor comprises the steps of forming a buried collector region, a base region and an emitter region in a device forming region surrounded by an isolation region, forming an impurity region contiguous to the buried collector region through an opening formed by etching away at least a portion of the isolation region, and forming a collector contact electrode in said opening in symmetry with a base contact electrode with respect to said emitter region.

Preferred embodiments of the invention described below provide: bipolar transistor wherein collision between the base region and the collector contact region may be effectively avoided to enable reduction or shrinking of the dimensions of the device to be achieved; and a process for preparing such a bipolar transistor with a higher efficiency. In the preferred bipolar transistors, a buried collector region, a base region and an emitter region are formed in a device forming region surrounded by an isolation region, an emitter region is formed by the intermediary of a semiconductor layer isolated by a side wall insulating layer, and a base contact electrode and a collector contact electrode are arranged in symmetry with each other.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which:

Figure 1 is a cross-sectional view of a bipolar transistor according to a first embodiment of the invention;

Figures 2a to 2e are cross-sectional views of the bipolar transistor at respective different stages during a step by step process for manufacturing it;

Figure 3 is a plan view of a second embodiment of the invention;

Figur 4 is a cross-sectional view taken along a line IV-IV in Figure 3;

Figure 5 is a cross-s ctional view of a third

embodiment of the invention; and

Figure 6 is a cross-sectional view of the above-described previously proposed bipolar transistor.

The bipolar transistor shown in Figure 1 comprises an N^+ type buried collector region 12 which is formed on a semiconductor substrate 11. An N type epitaxial layer 13 is formed on the buried collector region 12. An isolation region 14 is formed adjacent to the N type epitaxial layer 13 by a selective oxidation process. The N type epitaxial layer 13 is a device forming region and is surrounded by the isolation region 14. A base contact electrode 15, covered by an insulating layer 19, is formed on the surface of the N type epitaxial layer 13, over the isolation region 14, so as partially to contact the surface of the layer 13. Similarly, a collector contact electrode 16 is provided in symmetry with the base contact electrode 15 with respect to an emitter region, and extends over the isolation region 14 and is covered by an insulating layer 19. The base contact electrode 15 has a terminal portion that contacts the N type epitaxial layer 13. In the region of contact between the terminal portion of the base contact region 15 and the N type epitaxial layer 13, a P^+ type graft base region 23 is formed by diffusion of impurifies from the base contact electrode 15. The graft base region 23 is contiguous with a P type intrinsic base region 20 formed on the major surface of the N type epitaxial layer 13. An N^+ emitter region 21 is formed within the intrinsic base region 20 so as to face the major surface of the layer 13. The emitter region 21 is connected to an emitter electrode (not shown) through a thin polycrystalline silicon layer 18 applied to a space between side walls 17, 17 formed on end surfaces of the base contact electrode 15, collector contact electrode 16 and insulating layer 19.

The collector contact electrode 16 is not connected to the N type epitaxial layer 13 in the vicinity of the side walls 17, but is connected to the buried collector region 12 through an opening 10 formed in the isolation region 14 towards the side thereof where the collector contact electrode 16 is formed. It is to be noted that the buried collector region 12 and the collector contact electrode 16 are electrically connected to each other through an N^+ type collector contact region 22 which is a high concentration impurity region formed in the N type epitaxial layer 13 between the buried collector region 12 and the opening 10 such that, as described later, the characteristics of the bipolar transistor may be improved.

The opening 10 is formed on a boundary surface which is inclined relative to the major surface and which is disposed between the isolation region 14 and the N type epitaxial layer 13. Although it is known to make an electrical contact or connection at a region previously isolated by the insulating region, the opening 10 is formed in the pr sent mbodiment through the isolation r gion 14. By providing the opening 10 in this manner, the opening 10 is shifted towards the isolation region 14 by a distance equal to 1_0, for example, as compared to the case shown in Figure 6 in which the collector contact or connection is made in the vicinity of a position corresponding to the side wall 17, similarly to the base contact or connection. Hence, the distance 1_1 between the intrinsic base region 20 and the collector contact region 22 may be selected to be larger by an amount corresponding to the thus-obtained distance 1_0. This results in prevention of collision between the intrinsic base region 20 and the collector contact region 22 for reducing parasitic capacitance and elevating the collector to base breakdown voltage. Also, since the intrinsic base region 20 and the collector contact region 22 are formed with the relatively large distance 1_1 between them, the impurity concentration of the collector contact region 22 may be increased in order to lower the collector resistance. This is favourable above all when reduction or shrinking of the dimensions of the device is aimed at.

It is unnecessary for the base contact electrode 15 and the collector contact electrode 16 to be arranged completely in symmetry with each other. Thus, the electrodes 15, 16 may be arranged so as partially to confront each other. The position of the opening 10 may be such that a sufficient distance may be obtained between it and the intrinsic base region 20, while the opening 10 may be extended through to the bottom surface of the isolation region 14. A PNP type transistor may naturally be employed as the bipolar transistor.

A process for manufacturing the bipolar transistor will now be described. It is possible, with the present process, effectively to avoid collision between the base region and the collector region to permit a bipolar transistor with improved device characteristics to be produced easily. The process will be described hereinbelow on a step by step basis with reference to Figures 2a to 2e.

First, as shown in Figure 2a, an N^+ type buried collector region 32 is formed on a semiconductor substrate 31, and a N type epitaxial layer 33 is formed or provided on the layer 32. An isolation region 34 is formed selectively on the N type epitaxial layer 33, for example by selective oxidation. After formation of the isolation region 34, the region 34 is planarised and the entire surface of the region 34 is covered with a chemical vapour deposition (CVD) SiO_2 film or layer 35. The surface of the N type epitaxial layer 33, which represents a device forming region, is covered by the CVD SiO_2 film 35. Then, a portion of the CVD SiO_2 film 35 disposed on the N type epitaxial layer 33 is removed for exposing a portion 36 of the surface of the epitaxial layer.

Then, as shown in Figure 2b, an opening 37 is formed by etching away a portion of the isolation region 34. The opening 37 may be formed simultaneously with etching of the film 35 to form the exposed surface portion 36 or it may be formed by a separate etching process. The opening 37 may, for example, be positioned on the boundary surface between the insulation region 34 and the N type pitaxial layer 33, which is inclined relative to the major surface. The area of the buried collector region 32 can be reduced by making the collector contact at this position. How ver, this positioning is only illustrative and the collector contact may be

made at any other position which will ensure a positive separation between the collector contact region and the intrinsic base region to be formed later. Thus, as an example of one alternative, the opening 37 may be formed so that the buried collector region 32 will exist directly at the bottom of the opening. As a further alternative, the impurity region contiguous to the buried collector region 32 may be formed on the bottom of the opening 37, such as by ion implantation, after the formation of the opening 37, with the exposed surface portion 36 being masked.

After formation of the opening 37, a polycrystalline silicon layer 38 is formed over the entire surface, as shown in Figure 2c. The opening 37 is filled with the polycrystalline silicon layer 38, the polycrystal silicon layer 38 then being contiguous with the N type epitaxial layer 33 at the exposed surface 36. The thus-formed polycrystalline silicon layer 38 may be planarised if necessary or if desired.

Then, using a resist mask, N type and P type impurities are selectively introduced by ion implantation into the polycrystalline silicon layer 38. Thus, an N type impurity for making collector contact is introduced into a part of the polycrystalline silicon layer 38 including the exposed surface portion 36 and the opening 37, and a P type impurity for making base contact is introduced into a part of the polycrystalline silicon layer 38 including the exposed surface portion 36 and not including the opening 37. After the impurities are selectively introduced in this manner, a CVD SiO_2 film 39 is deposited over the entire surface of the polycrystalline silicon layer 38.

Then, using a mask as required, an opening for an emitter is formed, as shown in Figure 2d. Thus, a collector contact electrode 41 composed of the part of the polycrystalline silicon layer 38 into which the N type impurity has been introduced is formed in symmetry with a base contact electrode 40 composed of the part of the polycrystalline silicon layer 38 into which the P type impurity has been introduced, with respect to an emitter region which will be formed in the next process step. Since the collector contact electrode 41 also fills the opening 37, collector contact may be made at the opening 37, so that the collector contact electrode need not be extended into contact with the N type epitaxial layer 33 at the exposed surface 36 of the N type epitaxial layer 33. The base contact electrode 40 makes contact at a terminal portion 40a thereof with the N type epitaxial layer 33, and the base contact region is formed by impurity diffusion from the terminal portion 40a.

Then, on that portion of the surface where the emitter opening is formed as described above, a CVD SiO_2 film is formed and then etched back to form side walls 42, 42. A thin polycrystalline silicon layer 47 is then formed between the side walls 42, 42 and a P type impurity is introduced into the layer 47.

Then, an annealing operation is carried out so that, as shown in Figure 2e, a P type base contact region 43 is formed by diffusion from the terminal portion 40a of the base contact el ctrode 40, while an intrinsic base region 44 is formed by diffusion from the thin polycrystallin silicon layer 47 into which the impurity has been introduced. Also, in the same step or in a separate step, an N^+ type collector contact region 46 interconnecting the buried collector region 32 and the collector contact el ctrode 41 is formed by impurity diffusion from the collector contact electrode 41 within the opening 37.

The N type impurity is then introduced to a high concentration into the thin polycrystalline silicon layer 47 and annealing is then carried out so that an emitter region 45 is formed in self-alignment with the intrinsic base region 44.

It is to be noted that the side wall 42 may be of a dual structure, which is highly effective, above all when a projection such as an oxide film exists in the vicinity of the side wall of the collector contact electrode 41. Any type of annealing, such as rapid thermal annealing, may be employed.

In accordance with the above-described process for preparing or manufacturing the bipolar transistor, a larger distance may be provided between the intrinsic base region 44 and the collector contact region 46 for reducing the parasitic capacitance and improving the collector to base breakdown voltage. In addition, the device area may be reduced for promoting integration and reduction or shrinking of the dimensions of the bipolar transistor.

Figures 3 and 4 illustrate the construction of a bipolar transistor having a trench-shaped isolation region. The construction is such that an N^+ type buried collector region 52 is formed on a semiconductor substrate 50 and an N type semiconductor crystal region 53 is formed on the N^+ type buried collector region 52. The N type semiconductor crystal region 53 represents a device forming region which is surrounded by a trench-shaped isolation region 51.

A base contact electrode 64 is formed on the surface of the N type semiconductor crystal region 53 so as partially to contact said surface and to overlie an insulating layer 61. The base contact electrode 64 is covered by an insulating layer 66. A collector contact electrode 65 is formed on the insulating layer 61 in symmetry with the base contact electrode 64, and is covered by the insulating layer 66. The collector contact electrode 65 is not in surfacial contact with the semiconductor crystal region 53 and has an end surface 62 covered by a side wall 63. A portion of the collector contact electrode 65 fills an opening 70 formed in a portion of the trench-shaped isolation region 51. The coll ctor contact electrode 65 is connected to an N^+ type collector contact region 57 formed in the semiconductor crystal region 53 as a continuation of the N^+ type buried collector region 52. A base contact region 55 is formed by diffusion on a portion of the semiconductor crystal region 53 contacted by th base contact electrode 64, with the electrode 64 acting as a surface of diffusion. An intrinsic bas region 54 is formed by diffusion with the side wall 63 acting as a mask and is connected to the base contact region 55. An emitter region 56 is similarly formed at the inner side of the intrinsic base region 54, using the same mask.

In the above-described bipolar transistor, a larger distance may be obtained between the intrinsic base

region 54 and the collector contact region 57, so that collision between the intrinsic base region 54 and the collector contact region 57 may be avoided so as to reduce the parasitic capacitance and improve the collector to base breakdown voltage. In addition, owing to the larger distance between the intrinsic base region 54 and the collector contact region 57, a higher impurity concentration of the collector contact region 57 may be realised with a lower collector resistance. A further advantage may be obtained when reduction or shrinking of the dimensions of the device components is aimed at.

Figure 5 illustrates a modification of the bipolar transistor shown in Figures 3 and 4. The same references are used in Figure 5 to designate parts or components which are the same as those shown in Figure 4 and the corresponding description will not be repeated.

The bipolar transistor shown in Figure 5 differs from that shown in Figure 4 as regards the structure of an opening 80 thereof. Thus, a side wall 81 formed of an insulating material is formed on the lateral wall of the opening 80, the inside of which is filled by a collector contact electrode 65. On a bottom 82 of the opening 80, a portion 83 of an N^+ type buried collector region 52 is connected to the portion of the collector contact electrode 65 which is defined by the side wall 81. In this modified bipolar transistor, isolation between the collector contact region 65 and the intrinsic base region 54 can be additionally ensured by the side wall 81 of the opening 80.

It is to be noted that the base contact electrode and the collector contact electrode need not be arranged completely symmetrically with each other, and that the bipolar transistor may also be a PNP type transistor.

Claims

1. A bipolar transistor comprising
a monocrystalline semiconductor body (11, 31, 50) on a surface of which an isolation region (14, 34, 51) is formed,
a device forming region (13, 33, 53) surrounded by the isolation region (14, 34, 51),
a buried collector region (12/22, 32/46, 52/57, 52/83) formed in a portion of the device forming region (13, 33, 53) within the semiconductor body (11, 31, 50),
a base region (20/23, 44/43, 54/55) facing a portion of a surface of the device forming region (13, 33, 53),
an emitter region (21, 45, 56) facing a portion of the surface of the device forming region (13, 33, 53) and surrounded by the base region (20/23, 44/43, 54/55),
a base contact electrode (15, 40, 64) extending from the isolation region (14, 34, 51) to above the device forming region (13, 33, 53) and connected to the base region (20/23, 44/43, 54/55) on the surface of the device forming region (13, 33, 53);
a collector contact electrode (16, 41, 65) formed over the isolation region (14, 34, 51) and arranged in symmetry with the base contact electrode (15, 40, 64) with respect to the emitter region (21, 45, 56), and
an opening (10, 37, 70, 80) formed at at least a portion of the isolation region (14, 34, 51) and interconnecting the buried collector region (12/22, 32/46, 52/57, 52/83) and the collector contact electrode (16, 41, 65).

2. A bipolar transistor according to claim 1, wherein the emitter region (21, 45, 56) is isolated from the base contact electrode (15, 40, 64) and the collector contact electrode (16, 41, 65) by a side wall insulating layer (17, 42, 63), and wherein the base region (20/23, 44/43, 54/55) is formed by an intrinsic base region (20, 44, 54) and a graft base region (23, 43, 55) interconnecting the intrinsic base region (20, 44, 54) and the base contact electrode (15, 40, 64).

3. A bipolar transistor according to claim 1 or claim 2, wherein the isolation region (14, 34, 51) has been formed by selective oxidation and the opening (10, 37, 70, 80) is formed through the isolation region.

4. A bipolar transistor according to claim 3, wherein the opening (10, 37) is formed to an inclined boundary surface between the isolation region (14, 34) and the device forming region (13, 33).

5. A bipolar transistor according to claim 1 or claim 2, wherein the isolation region (51) is a trench-shaped insulation layer and the opening (70, 80) is formed at a side of the insulating layer towards the device forming region (53).

6. A bipolar transistor according to claim 5, wherein an insulating layer (81) is formed on a side wall of the opening (80) and the opening (80) is contacted only at the bottom (82) thereof by the buried collector region (52/83).

7. A process for manufacturing a bipolar transistor, the process comprising:
forming a buried collector region (32) in a device forming region (13) surrounded by an isolation region (34) of a monocrystalline semiconductor body (31);
forming a base region (44/43) and an emitter region (45) surrounded by the base region on a surface of the device forming region (33);
forming an impurity region (46) through an opening (37) formed by etching off at least a portion of the isolation region (34), the impurity region (46) being contiguous to the buried collector region (32); and
forming in the opening (37) a collector contact electrode (41) arranged in symmetry with a base contact electrode (40) with respect to the emitter region (45).

8. A process for manufacturing a bipolar transistor, the process comprising:
forming a buried collector region (32) in a monocrystalline semiconductor substrate (31);
producing an epitaxial layer (33) on the monocrystalline semiconductor substrate (31);

forming a mask selectively on the epitaxial layer (33), which layer acts as a device forming region, and also forming an isolation region (34) surrounding the device forming region (33) by selective oxidation;
forming an insulating film (35) over the entire surface;
forming an opening (37) in a portion of the device forming region (33);
forming a semiconductor layer (38) on the entire surface including the opening (37);
introducing an impurity into the semiconductor layer (38) so that the layer has different conductivity types as between a first region thereof and a second region thereof which is arranged in symmetry with the first region and includes the opening (37);
partially removing the semiconductor layer (38) so that it is divided to form contact electrodes (40, 41) corresponding to the first and second regions of different conductivity types and so that the device forming region (33) is exposed; and
forming a side wall insulating layer (42) where the semiconductor layer (38) was removed and forming an emitter region (45) contiguous with a surface of the side wall insulating layer (42).

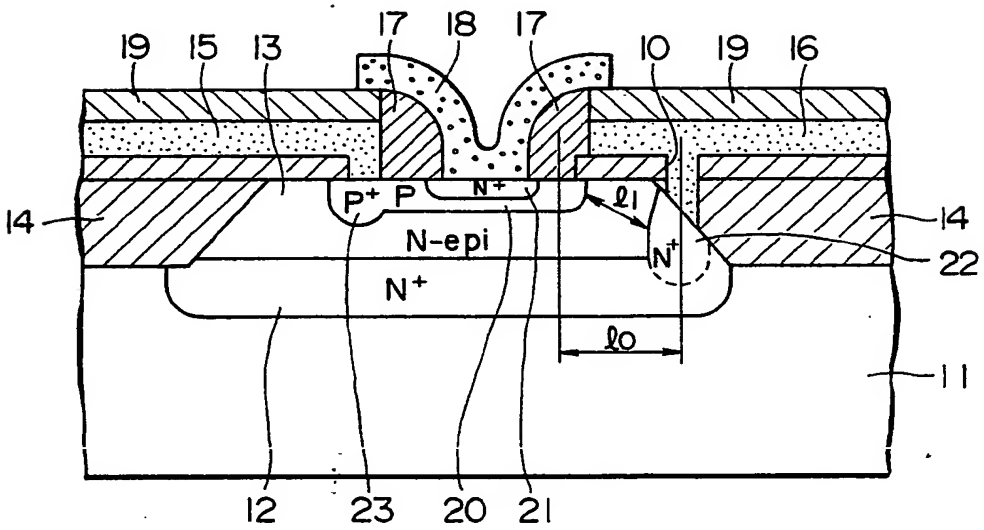

FIG.1

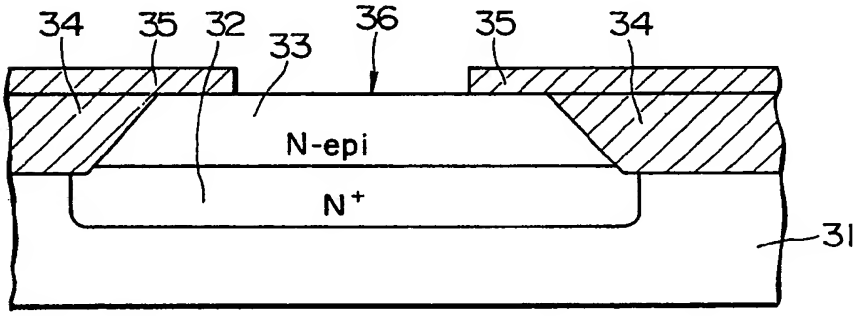

FIG.2a

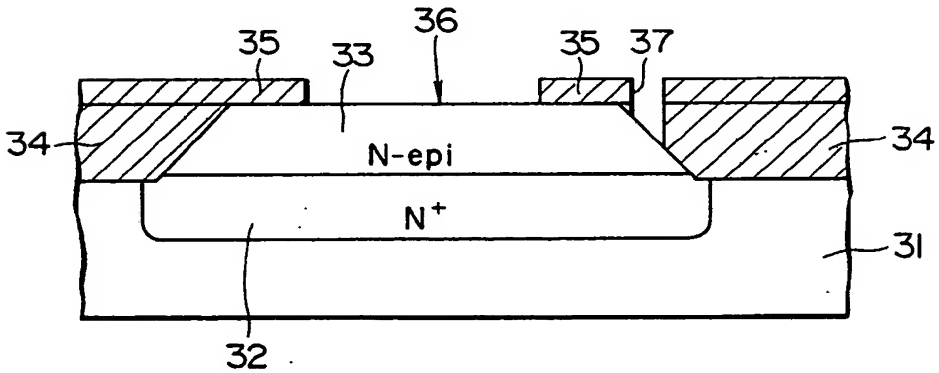

FIG.2b

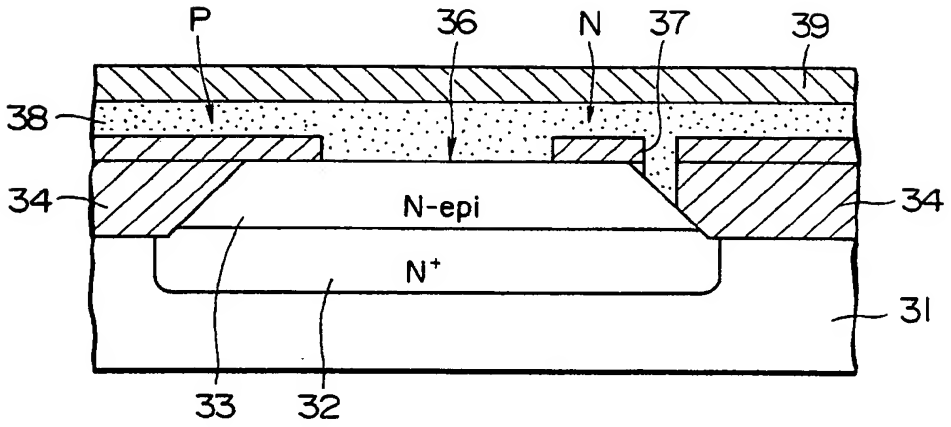

FIG.2c

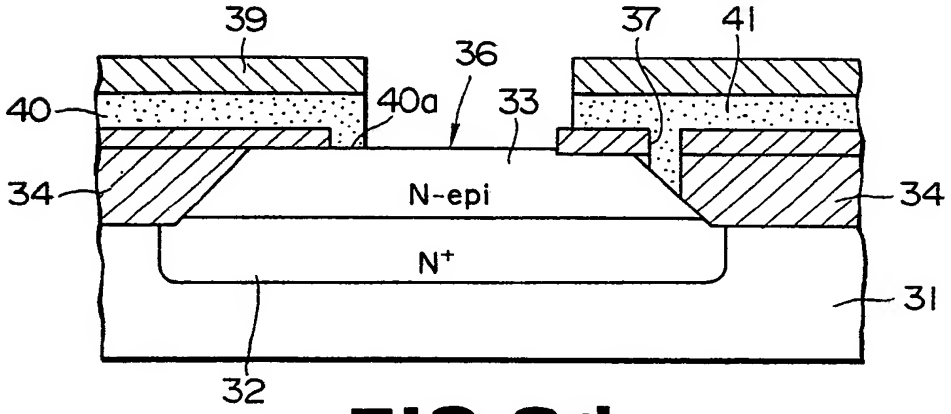

FIG.2d

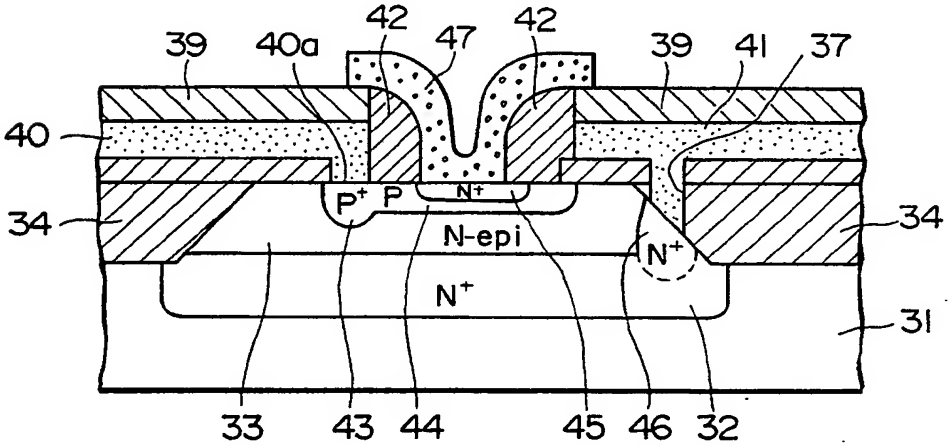

FIG.2e

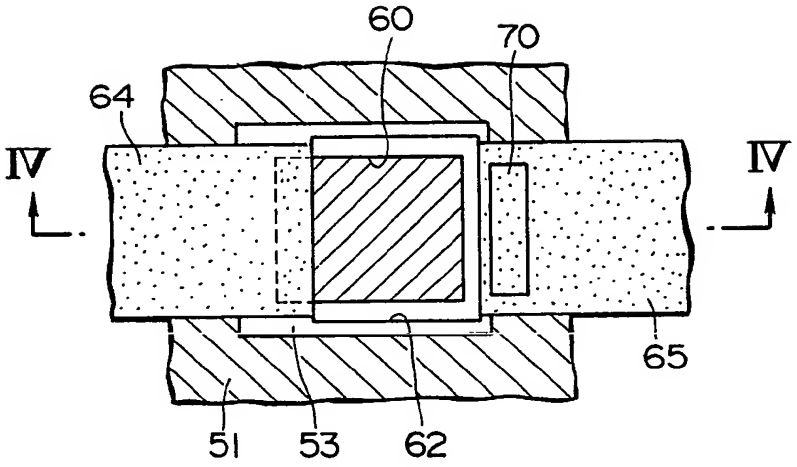

FIG. 3

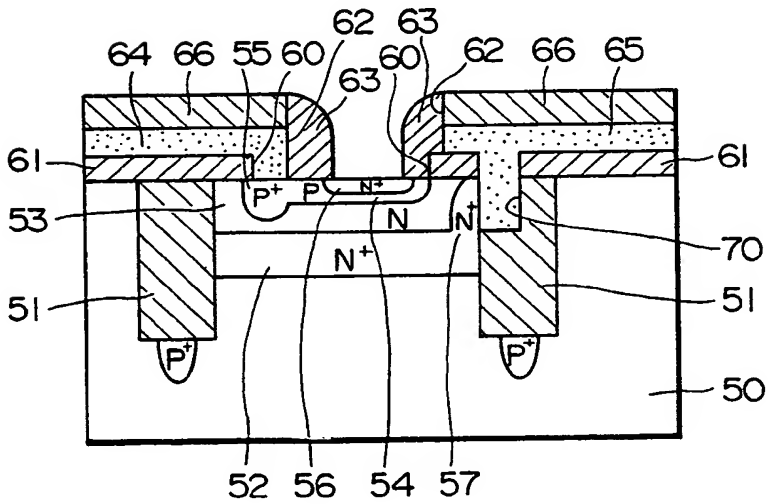

FIG. 4

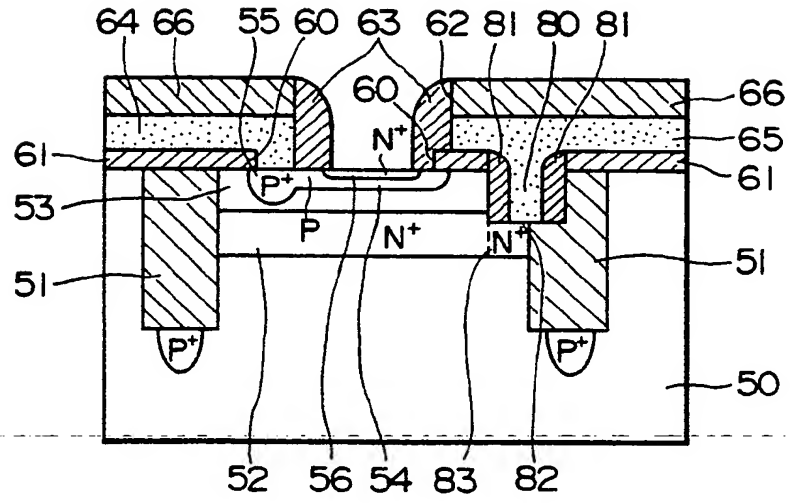

FIG.5

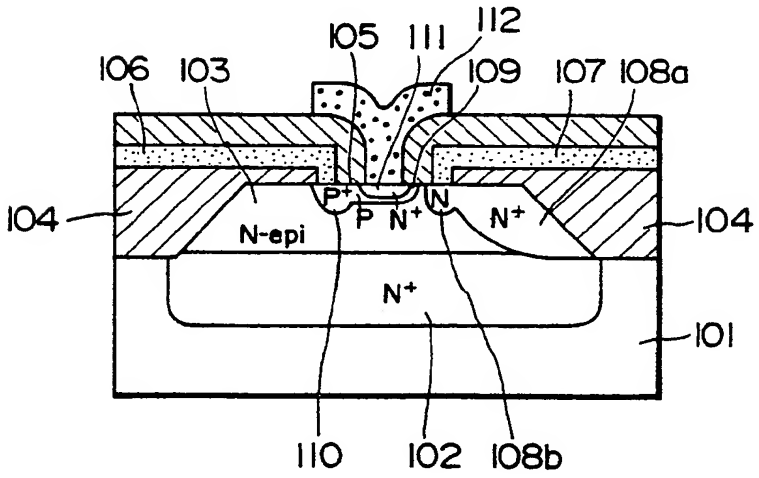

FIG.6

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 303 435**
A3

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **88307335.5**

(51) Int. Cl.4: **H01L 29/52 , H01L 29/60**

(22) Date of filing: **08.08.88**

(30) Priority: **11.08.87 JP 199006/87**

(43) Date of publication of application:
15.02.89 Bulletin 89/07

(84) Designated Contracting States:
DE FR GB NL

(88) Date of deferred publication of the search report:
03.01.90 Bulletin 90/01

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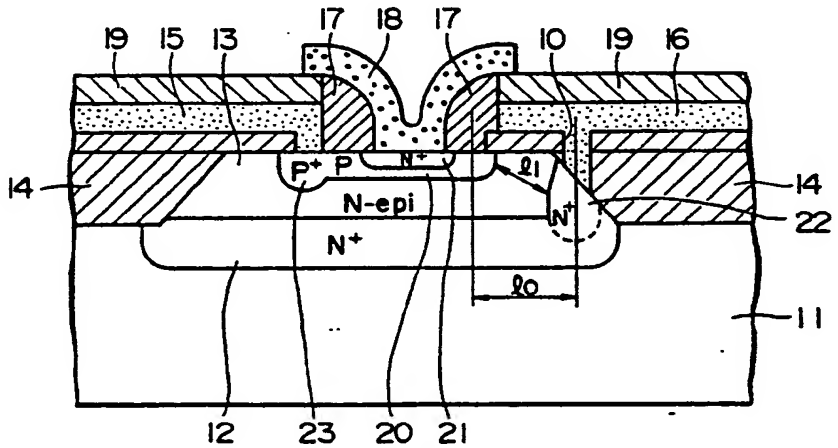

FIG.1

EP 0 303 435 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 30 7335

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X Y A	EP-A-0 144 444 (SONY CORP.) * Abstract; figures 3A-3M; page 2, line 15 - page 3, line 24 *	1,7 1,3 8	H 01 L 29/52 H 01 L 29/60
Y	US-A-3 534 234 (L.H. CLEVENGER) * Whole document *	1,3	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26-09-1989	MIMOUN B.J.

CATEGORY OF CITED DOCUMENTS

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